

What is claimed is:

1 1. A feedback control I/O buffer driven by a system
2 voltage, comprising:
3 an input/output circuit comprising a first PMOS
4 transistor and a first NMOS transistor and having
5 an I/O port coupled to an I/O pad, wherein the first
6 PMOS transistor has an N-well region, a gate of the
7 first NMOS transistor receives a first gate control
8 signal, and a drain of the first PMOS transistor
9 serves as the I/O port;
10 a N-well control circuit coupled to I/O pad to control
11 the voltage level at the N-well region of the first
12 PMOS transistor according to the feedback signal
13 output from the inverter; and
14 a P-gate control circuit receiving a second gate control
15 signal and being output to the gate of the first
16 PMOS transistor, wherein the P-gate control
17 circuit comprises:
18 a transmission gate having a second NMOS transistor
19 and a second PMOS transistor, the sources of
20 which are coupled to the second gate control
21 signal, and the gates of which are coupled to
22 the system voltage and the N-well control
23 circuit respectively; and
24 a third PMOS transistor having a drain and a source
25 coupled to the gate and the floating N-well
26 region of the first PMOS transistor
27 respectively, and a gate coupled to the system
28 voltage.

1 2. The feedback control I/O buffer as claimed in Claim
2 1, wherein the N-well control circuit adjusts the voltage
3 level at the N-well region of the first PMOS transistor to
4 the voltage level of the input voltage when the input voltage
5 exceeds the system voltage.

1 3. The feedback control I/O buffer as claimed in Claim
2 2, wherein the N-well control circuit adjusts the voltage
3 level at the N-well region of the first PMOS transistor to
4 the voltage level of the system voltage when the input voltage
5 is lower than the system voltage.

1 4. The feedback control I/O buffer as claimed in Claim
2 1, wherein the input/output circuit further comprises a fourth
3 NMOS transistor having a source and drain coupled to the I/O
4 pad and the drain of the first NMOS transistor respectively,
5 and a gate coupled to the system voltage.

1 5. The feedback control I/O buffer as claimed in Claim
2 4, wherein the N-well control circuit comprises:

3 a fourth PMOS transistor having a source coupled to the
4 I/O pad, a gate coupled to the system voltage, and
5 a drain coupled to the N-well region of the first
6 PMOS transistor;

7 a fifth PMOS transistor having a gate coupled to the
8 system voltage, a source coupled to the I/O pad,
9 and a drain;

10 a sixth PMOS transistor having a gate coupled to the drain
11 of the fifth PMOS transistor, a drain coupled to
12 the system voltage, and a source coupled to the
13 N-well region of the first PMOS transistor; and

14 a fourth NMOS transistor having a source and drain
15 coupled to the I/O pad and the gate of the sixth
16 PMOS transistor, and a gate coupled to the system
17 voltage.

1 6. An input/output buffer, comprising:
2 a floating N-well;
3 a first NMOS transistor having a gate coupled to a first
4 gate control signal, and a source coupled to the
5 ground;
6 a second NMOS transistor having gate coupled to a system
7 voltage, a source coupled to a drain of the first
8 NMOS transistor and a drain coupled to an I/O pad;
9 a third NMOS transistor having a gate coupled to the
10 system voltage, and a drain coupled to the I/O pad;
11 a first PMOS transistor having a source coupled to the
12 system voltage, and a drain coupled to I/O pad;
13 a second PMOS transistor having a source coupled to the
14 I/O pad, a gate coupled to the system voltage, and
15 a drain coupled to floating N-well;
16 a third PMOS transistor having a source coupled to I/O
17 pad, a gate coupled to the system voltage, and a
18 drain coupled to a source of the third NMOS
19 transistor;
20 a fourth PMOS transistor having a gate coupled the drain
21 of the third PMOS transistor, a drain coupled to
22 the system voltage, and a source coupled to the
23 floating N-well;
24 a transmission gate including a fifth PMOS transistor
25 and a fourth NMOS transistor, wherein the sources

26 of which are coupled to a second gate control
27 signal, the drains of which are coupled to the gate
28 of the first PMOS transistor, and the gates of which
29 are coupled to a drain of the third PMOS transistor
30 and the system voltage respectively; and
31 a sixth PMOS transistor having a gate coupled to the
32 system voltage, a drain coupled to the gate of the
33 first PMOS transistor and a source coupled to the
34 floating N-well and the source of the fourth PMOS
35 transistor; wherein the floating N-well is
36 connected to the substrate on which the first to
37 sixth PMOS transistors are formed.